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THESIS

SAMPLE FABRICATION AND EXPERIMENTAL DESIGN FOR STUDYING INTERFACIAL CREEP AT THIN FILM / SILICON INTERFACES

by

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March 2004

Thesis Advisor: **Indranath Dutta**

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SAMPLE FABRICATION AND EXPERIMENTAL DESIGN FOR STUDYING INTERFACIAL CREEP AT THIN FILM / SILICON INTERFACES

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ABSTRACT

This thesis developed the sample fabrication and experimental design for studying interfacial creep at thin film / Silicon interfaces. The specific interface of study was the crystalline interface created by Positive Vapor deposition of a metallic thin film on a very smooth Silicon substrate. Emphasis was placed on development and refinement of the fabrication techniques necessary to produce test samples that provide valid reproduction of the interfacial stress state in isolation from other stresses inherent in the complete device. Test sample fabrication utilized traditional laboratory methods combined with leading edge methodology in two fabrication steps; namely diffusion bonding of an Silicon substrate / PVD Aluminum thin film / Silicon substrate composite structure and micro-machining Silicon through the use of a TMAH based etchant. In conjunction with the sample development a test platform was designed, fabricated, assembled, and aligned to provide for isolated parametric characterization of the proposed interfacial creep model. The results of this characterization are anticipated to be of significant utility in improving the design for fabrication and reliability of current and next generation microelectronic and microelectro-mechanical devices.

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For Peter Grenville Thornell.

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I. INTRODUCTION

Rapid developments in the design and manufacturing technology of electronic devices have occurred over the last half-century. The transitions from electron tube based discrete component circuits to P-N junction transistor based discrete component circuits to Silicon based integrated circuit chips have ushered in a new era of miniaturization. With each generation of development the component density has increased from circuits per square meter to circuits per square centimeter to circuits per square millimeter. Fueling this development has been our rapid expansion of utility for ever smaller and more capable devices. Indeed, the proliferation and rapid expansion of computing technology has enabled us to synergistically utilize the components developed in the current generation to design and manufacture the smaller and more functionally dense components of the next generation. As these new devices are developed in a technologically hungry and consumer driven marketplace, the constant competitive necessity of those who design and manufacture them is to increase miniaturization of the overall device while expanding its functional capacity.

Classical understanding of the bulk behavior of polycrystalline materials, from which the early generations of electronic components were manufactured, was adequate for their design and fabrication. As the size of these components and their constituent subcomponents has reduced dramatically, the applicability of bulk polycrystalline material characteristics in modeling their behavior has become increasingly inaccurate in predicting their actual behavior. In many cases, the design and fabrication of current generation microelectronic and microelectro-mechanical devices has preceded the full understanding of the micro scale behavior of their constituent components and of the interfaces that join them. Classical joining technology such as bolts and rivets on the meter scale has given way to vapor deposition and diffusion bonding in the micrometer scale. Advanced understanding of this micro scale behavior is increasingly critical in the regions of interface between two materials of micro scale.

Component miniaturization, enabled by micro scale fabrication methods, has, in many instances, preceded our full understanding of the behavior of the materials and

devices. This is especially true in the interface region. Classical bulk polycrystalline behavior of the materials at the interfaces most critical to the design for fabrication and long-term reliability has been shown to be no longer valid in predicting the behavior of the subcomponent materials at these critical interfaces. Our ability to design and fabricate devices having reliable long-term utility has become increasingly dependent upon operational testing of experimentally fabricated devices. As the costs of experimental fabrication and testing of components has increased in proportion to their complexity and in inverse proportion to their size, the need for improved understanding of their interfacial behavior to support predictive modeling has also grown.

Periods of large thermal deviation occur in both the fabrication and operation of micro-scale electronic devices. These temperature changes produce high interfacial shear stress states at the subcomponent interfaces due to coefficient of thermal expansion differences of the interfacing materials. Frequently this occurs with at least one of the constituent materials at high homologous temperature. The response of thin films to this shear loading is likely to differ greatly from that expected for bulk polycrystalline material. Diffusionally accommodated interfacial creep at activation energy levels well below those observed in bulk polycrystalline materials has been observed in, metal-metal composites, and metal-Si interfaces [6-11]. In thin film / substrate systems, results as significant as alteration of the film footprint on the substrate material have been observed [1,2,3]. This thin film interfacial behavior has been described in several manners but not experimentally isolated and parametrically tested to develop and validate a fully characterized model [4,5].

Recent research into the behavior of the diffusion bonded interface between Silicon and Aluminum has shown excellent correlation to an interfacial creep model and led to the parameterization of that model for the regions of homologous temperature under which the current generation of micro electrical and microelectro-mechanical devices are stressed [6]. The measured kinetics of that investigation showed that the mechanism of sliding is interfacial diffusion-controlled diffusional flow. The measured kinetics also showed an inversely varying relationship to the square of the interfacial roughness, indicating that smooth surfaces such as those involved in microelectronic devices are highly susceptible to sliding with activation energies of approximately half as

much as the activation energy for volume diffusion. Further analysis also revealed that the region for creep was contained within a very thin interfacial with no observed deformation of either material adjoining the interface [6,8]. The process appeared to have been assisted by the presence of a a very thin omrphous interfacial zone, possibly created during diffusion bonding of Al ans Si. These results [6-8] spurred the desire to investigate wether interfaces formed by the Physical Vapor Deposition (PVD) of a thin film on a substrate (e.g., Al on Si) are also susceptible to interfacial sliding. Because of the importance of such interfaces in a wide range of applications, e.g., Microelectronics, MAMS, etc., and the potential impact of interfacial sliding on the reliability of components, the study conceptualized here is expected to be valuable.

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II. BACKGROUND

Interfacial creep is the sliding between adjoining bonded constituents by a diffusionally accommodated mechanism. This sliding occurs without fracture of the interface or the constituents. Thus, the interface retains its full bond while thermal and stress driven diffusional processes cause mass transport of material in one or both of the constituents, resulting in relative motion at the interface without de-bonding or frictional sliding [9,10,11,12]. For interfacial creep processes to occur two requirements must be met at the interface. First, a shear stress must exist at the constituent interface; this provides the stress gradient necessary for directional mass transport. Second, a high homologous temperature, of at least one of the constituent components, must exist; it enables the diffusion of atoms of that material to occur at appreciable rates. Both requirements one and two are met during the fabrication and operational environments of current generation micro electrical and microelectro-mechanical devices having PVD metallic thin film / silicon substrate interfaces. A third condition has also been observed that has been shown to be of significant effect on the interfacial creep kinetics of some interfaces. In investigation of the diffusion bonded Aluminum / Silicon interface a thin amorphous interfacial layer was observed. This layer was observed to provide a path for rapid diffusional mass transport to which all observed displacement was constrained with no evidence of interfacial decohesion or bulk lattice distortion of either constituent [6,7]. The presence of this third condition has not been found at all thin film / substrate interfaces; however its presence has been found to be significant at the diffusion bonded interfaces where it was found.

A. PREVIOUS RESULTS OF INTERFACIAL CREEP STUDIES

1. Microelectronics

Interfacial sliding has been observed to occur in microelectronics thermal cycling tests at temperatures well below those anticipated to cause creep based upon macroscopic material properties [1,2,6,8,10,11,12]. Current research into this phenomenon has shown motion of metal film lines due to thermal cycling to occur in ratcheting steps with each

thermal cycle. These steps, deemed crawling [1], show displacement of films towards the die center with accumulated displacement maximum at the edges of the die and gradually reducing towards the center of the die. Regardless of the naming convention, the excessive deformation of these metal films is an important failure mode in current generation microelectronics needing immediate research. Figure 1 shows a schematic of a part of metallic thin film interconnect on a Silicon substrate and a micrograph of that same structure after being thermally cycled. This figure clearly demonstrates the detrimental effects of interfacial creep on the design for fabrication and long-term reliability of current generation microelectronic devices.

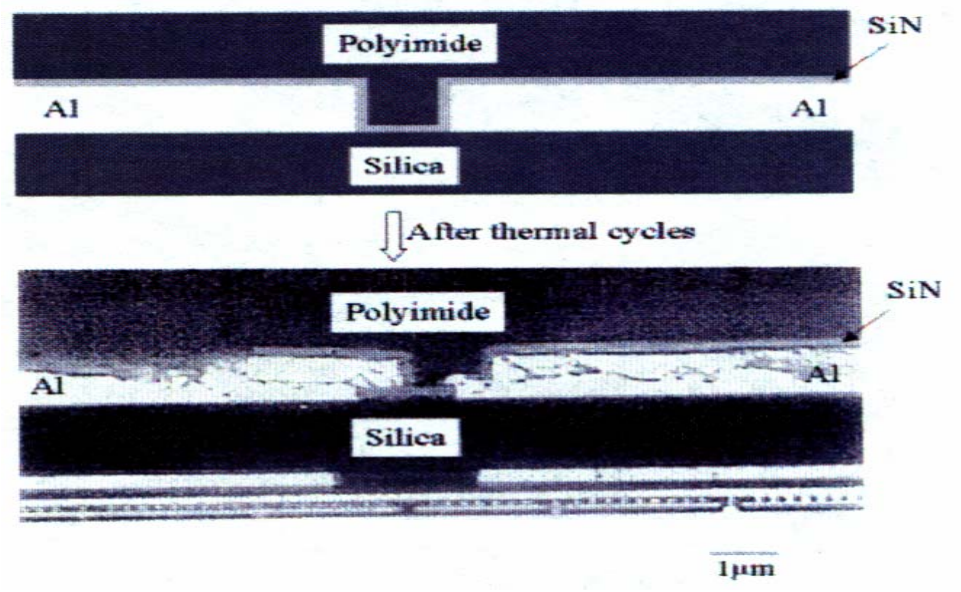

Figure 1. A schematic of a part of an interconnect structure before thermal cycling, and a micrograph of the same structure after thermal cycling. [From Ref 1]

Interfacial sliding by diffusional mechanisms has also been observed in copper/polyimide high density interconnects (HDIC) on silicon during thermal cycling [13,14]. Evaluation of the impact of one such thermal cycle by atomic force microscopy (AFM) of the surface of a single HDIC layer showed sliding along the vertical Cu-Ta interfaces resulting in a significant change in the relative heights of the PI and Cu lines. Figure 2a shows a schematic of Cu/PI HDIC on Si with Ta Interlayers. Figure 2b shows the relative height difference between the PI and Cu layers due to one thermal cycle. This has been attributed to diffusionally accommodated sliding driven by shear stresses

generated by the large Coefficient of Thermal Expansion mismatch (ΔCTE) between the PI, Ta and Cu layers in the out-of-plane direction.

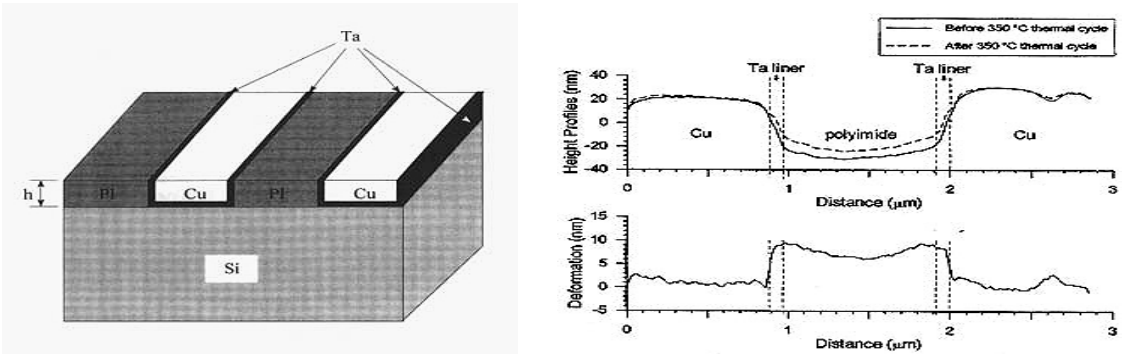

Figure 2. (a) Schematic of Cu/PI HDIC on Si with Ta Interlayers. (b) Surface Profile Before and After Thermal Cycling, and Plot Showing Differential Deformation of Cu and PI via Sliding at Cu/Ta Interface [From Ref 13].

Sliding has been shown to occur in the in-plane (horizontal) direction and out of plane (vertical) direction depending upon the stress state and constraints of the physical device. The substantial ΔCTE between metal and Si (~$21x10^{-6}$/K for Al-Si) results in very large in-plane stresses in thin film interconnects during fabrication steps and normal device operation. Figure 3 shows schematically the interfacial shear stress distribution along the width of a metallic thin film line when placed in in-plane biaxial tension due to a temperature change. Together, the high stress and high homologous temperature can activate creep mechanisms in metallic thin film interconnects at homologous temperatures below those anticipated for creep based on macroscopic bulk properties.

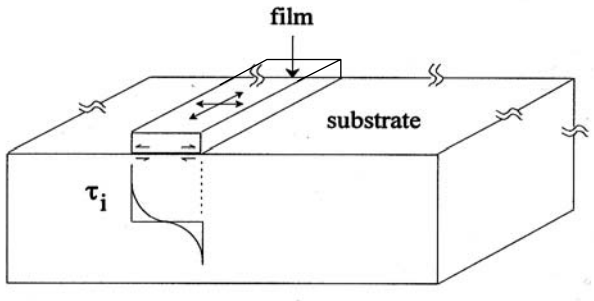

Figure 3. Schematic of Interfacial Shear Stress Distribution along the Width of a Narrow Thin-Film Line. The Film is in In-Plane Biaxial Tension. [From Ref 2]

Direct analytic study of the kinetics of interfacial sliding is difficult with complete components from industry. The complexity of these components and the multitude of interfaces and materials involved produces highly complex stress states with potentially competing mechanisms of subcomponent interaction. Superposition of several competing phenomena produces results that are neither uniformly applicable nor independently determinable in isolation from concurrent effects. To understand these complex systems we must first understand the individual kinetics of each individual interface under simple loading conditions.

2. Metal Matrix Composites

Slow thermal cycling of many metal matrix composites have shown vivid evidence of interfacial creep with no debonding of the interface. Slow thermal cycling of graphite fiber reinforced aluminum matrix composites [9,11], resulted in matrix protrusion past the fiber ends. Slow heating / cooling rates in conjunction with the tensile matrix thermal stress along the fiber-axes, allowed the matrix to elongate relative to the fibers with no interfacial debonding. The ΔCTE between the matrix and fibers creates large interfacial shear stresses at the fiber ends that, over time, was accommodated for by diffusional sliding of the interface. Figure 4 shows micrographs of the significant interfacial creep results form these two studies.

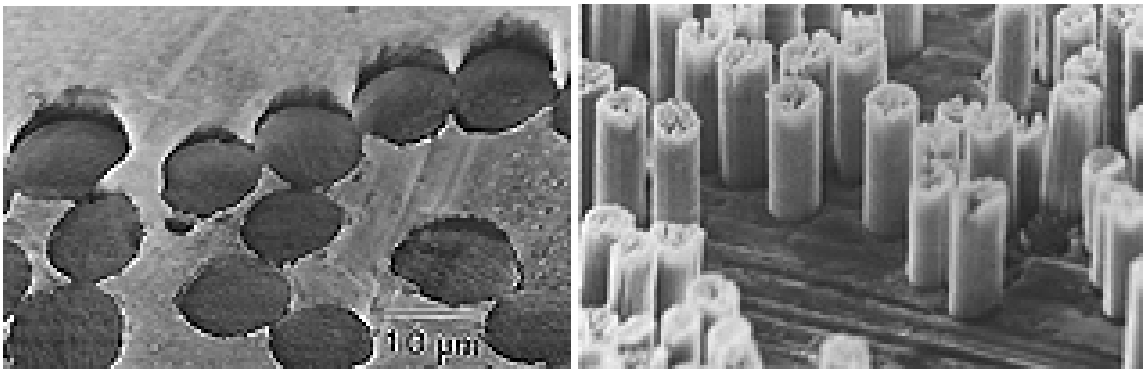

Figure 4. Intrusion and Protrusion of Graphite Fiber-Ends Relative to an Al-Matrix Following Slow Thermal Cycling from 298K to 380K and 600K, Respectively [From Ref 9, From Ref 11].

B. CHARACTERIZATION OF INTERFACIAL CREEP

Direct analytic study of the kinetics of interfacial sliding is difficult with complete components from industry. Multi cycle analyses of operating components (i.e., comparisons of changes in the component structure from fabrication through 1, 10, 100, 1000 etc. operating cycles) show the net result of multiple superposed phenomena but yield unisolable interaction kinetics results of the individual phenomena. The complexity of these components and the multitude of interfaces and materials involved produces highly complex stress states with potentially competing mechanisms of subcomponent interaction. Superposition of multiple competing phenomena produces results that are neither uniformly applicable nor independently isolable. In order to circumvent these difficulties, Funn and Dutta [10] designed experiments and analytical approaches, to study the kinetics of interfacial creep in isolation from other superimposed phenomena, and measured the kinetics of interfacial sliding in Pb-Ni and Pb-SiO_2 single fiber composites. An interface-sliding model was proposed using a diffusional creep law with a threshold stress and an activation energy corresponding to interfacial diffusion. This model is further discussed in section C.

C. DIRECT MEASUREMENT OF INTERFACIAL CREEP KINETICS

Previous studies of two single filament composite system models [10,11] isolated and directly measured the kinetics of interfacial sliding at the matrix-fiber interface. Findings of those studies show that the interfacial sliding was described by diffusional flow with a threshold stress. Further analysis performed in those studies also revealed by Scamming Electron Microscopy (SEM) that the surface morphology of the interface played a key role in creating a periodically varying stress state at the interface when subjected to far-field shear and normal stresses. Recognition of the fact that the interfacial surface morphology can never be truly smooth is a significant key to the development of this model.

To describe the interfacial topography a simple model based upon periodic variance of the interfacial relief, y, of either constituent can be applied as:

$$y = \frac{h}{2}\cos\left(\frac{2\pi x}{\lambda}\right)$$

Where x is the in-plane and y is the out-of-plane position of the interface, h is the amplitude of topographical relief and λ the periodicity of peak-to-peak occurrence along the interface.

Variation in the interface due to interfacial surface morphology of the constituent components creates localized variation of the interfacial stress state. This variation creates localized stress cells at the interface when far field shear and normal stresses are applied. Figure 5 shows graphically how localized variation in the surface morphology results in localized variation of the stress state. To model this variation a periodic interface morphology model was adapted to quantifiably explain the interface morphologies role in creating localized stress variation along the interface aiding the diffusion mass transport of the diffusing species.

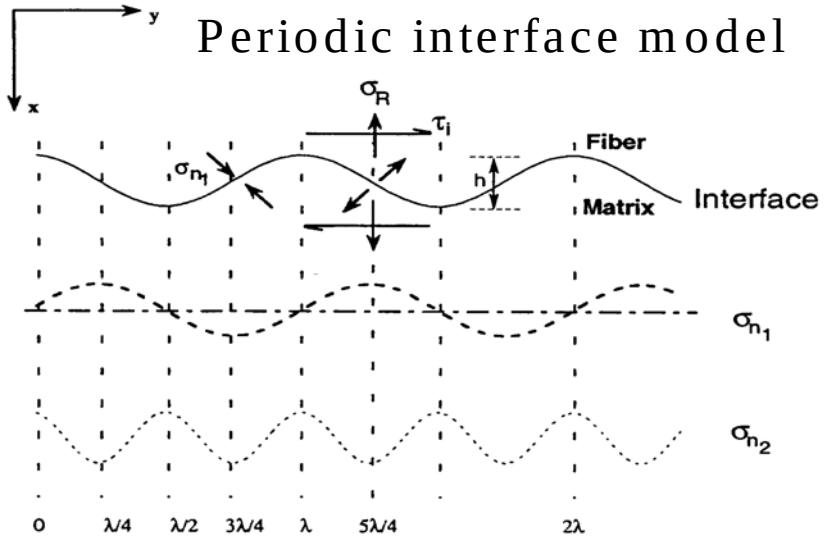

Figure 5. Periodically varying interface due to surface morphology and the effect on local interfacial stresses when subjected to far field shear and normal stresses [From Ref 10].

Funn and Dutta [10] showed experimentally that interfacial sliding in the absence of adhesive failure may be described by a diffusional creep law with a threshold stress and an activation energy corresponding to interfacial diffusion. They proposed that

sliding occurs by interface-diffusion-controlled diffusional creep, with contributions from both shear (τ_i) and normal stresses (σ_i) acting on the interface, with the sliding strain rate $\dot{\gamma}_i$ being given by:

$$\dot{\gamma}_i = \frac{4\delta_i D_{io}\Omega}{kTh^3}\left[\tau_i + 2\pi^3\left(\frac{h}{\lambda}\right)^3\sigma_i\right] \exp\left[-\frac{Q_i}{RT}\right]$$

Where δ_i is the thickness of the interface, Q_i and D_{i_o} are the activation energy and frequency factor, respectively, for interfacial diffusion, Ω is the atomic volume of the diffusing species (i.e., film material), λ and h are the morphological periodicity and roughness, as shown in Figure 5, of the interface, and k, R and T are the Boltzmann's constant, Gas constant, and absolute temperature, respectively.

Analysis of the stress parameter shows how this model explains the occurrence of interfacial sliding at temperatures below those where creep would macroscopically be expected to occur. Both shear and normal stresses at the interface contribute to the periodically varying interfacial stress that depends strongly on the interfacial roughness parameter h/λ. A compressive σ_i reduces the effective interfacial stress resulting in threshold behavior and slows the creep rate while a tensile σ_i increases the effective interfacial stress and speeds the creep rate.

D. DIRECT MEASUREMENT OF DIFFUSION BONDED INTERFACIAL CREEP KINECTICS

Petersen, Dutta, and Chen [2,6,7] isolated the Aluminum / Silicon Diffusionally bonded interface and performed direct measurements of the Interfacial sliding creep kinetics of that interface via implementation of a double shear test sample. Figure 6 shows the fabricated double shear test sample and loading scheme employed for measurement of Interfacial creep kinetics of the Al / Si diffusion bonded interface.

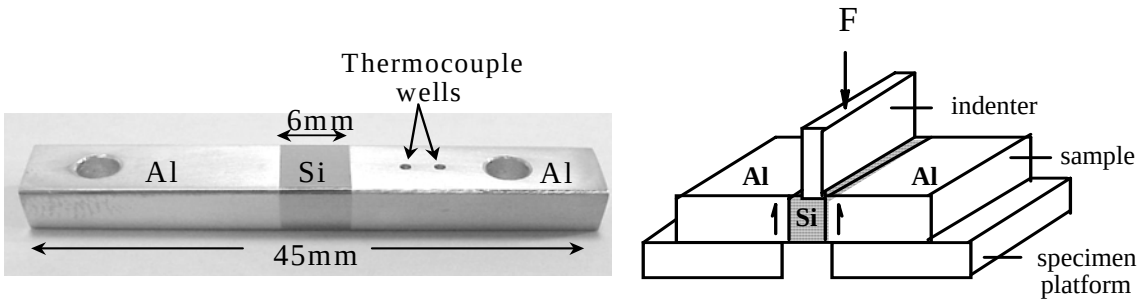

Figure 6. Photo of Double Shear Diffusion Bonded Interfacial Creep Test Specimen (a), and Schematic of the Loading Geometry employed in kinetics testing (b) [From Ref 6].

In preparation of Al / Si / Al diffusion bonded test samples multiple Silicon and Aluminum constituent components of varied but controlled interfacial surface morphology were fabricated. The effects of each combined surface morphological mating were studied on the resultant interfacial morphology of the diffusion bonded test sample and then measured by constant stress creep tests at high homologous temperature of the Aluminum to determine the creep kinetics of each interface.

Inspection of the various interfaces created [2,7,8] by optical, scanning electron microscopy, orientation imaging microscopy, and transmission electron microscopy showed that the more ductile species (Al) underwent intense localized deformation during the bonding process resulting in an interfacial morphology characterized by the initial morphology of the harder species (Si). This deformation also produced an Oxygen rich amorphous region at the interface composed of randomly oriented Al atoms whose thickness varied somewhat across the breadth of the interface but whose minimum thickness was consistent with the measured value of h of the Si surface morphology [7]. Bonding success was found to be dependent upon the more ductile species (Al) having a surface morphology that was able to fill the interstities and asperities of the less ductile component while dispersing the surface oxide films of the two components at a temperature below the eutectic temperature of the binary phase diagram of the two

constituents. The bond produced a sharp interface on the Si side of the bond and an amorphous O-rich region on the Al side of the bond whose thickness varied somewhat over the breadth of the specimen but whose minimum thickness correlated well with the surface morphology (h) of the harder Si as measured prior to bonding.

In performance of creep tests Peterson, Dutta, and Chen [2,6] validated the interface diffusion controlled diffusional creep model for interfacial sliding. Three key results were obtained. First, they showed that the creep rate decreases sharply with increase of interfacial roughness (h) while retaining linear stress dependence for all successfully fabricated interfacial morphologies. Second, they showed that all deformation observed from each tested sample was confined to the interface with negligible deformation of the Si or Al material outside the interfacial region. No evidence of interfacial de-cohesion, grain textural change or lattice curvature outside of the amorphous interfacial region were observed while uniform displacement of the Si and Al were observed along the entire interface. Suggesting that the amorphous layer that lies at this interface acts as an effective conduit for diffusional flow. Third, the effect of far field normal stress, independent of temperature, produces a threshold temperature. Thus:

$$\tau_{eff} = \tau_i - \tau_o \quad \text{where:} \quad \tau_o = 2\pi^3 \left(\frac{h}{\lambda} \right)^3 \sigma_n$$

Creep, occurring after threshold levels are exceeded, with the same level of activation energy (Q=42 kJ/mole) as found in sample tests not subjected to far field normal stresses.

These conclusions again validated the interface diffusion controlled diffusional creep model for interfacial sliding and with activation energies of half their value for bulk material. The success of these experiments, and the obseervation that their amorphous zone present at the interface influences sliding, stimulated further investigation into the kinetics of the PVD Aluminum Thin film / Silicon interface that are the basis of this research project, particularly, in order to ascertain whether interfacial sliding is significant even when there is no amorphous zone.

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III. OBJECTIVES

The objective of this research is to develop a methodology for isolating and directly studying the kinetics of interfacial creep at metallic thin film / Silicon substrate interfaces. The interface to be tested must be isolated in single shear to preclude the application of multi-axial stresses on the interface, and to prevent deformation of the metallic thin film, so that any observed displacement between the metallic thin film and the Si substrate can be directly attributed to interfacial sliding. The PVD metallic thin film must be of a similar thickness as metallic interconnect lines used in current generation devices to be of value in current and next generation development of microelectronic and electro-mechanical devices [15]. The fabrication methods employed, while at a laboratory level, must accurately match the metallurgical conditions at the interface of industry-produced interfaces in the current manufacturing processes. The materials from which the test devices are constructed must be relevant to ongoing fabrication technology and possess limited mutual solid solubility. With this in mind, the primary focus of this thesis is to develop a design and fabrication approach for samples suitable for testing of interfacial sliding kinetics in the Si substrate – Al thin film system.

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IV. EXPERIMENTAL METHODOLOGY

A. PHYSICAL SPECIMEN DESIGN AND FABRICATION

Two competing, but not mutually independent, requirements of the physical specimen are that first a thin film of the same order of magnitude as that employed in the production of current generation microelectronic and microelectro-mechanical devices and second that the test specimens be of physical size adequate for easy handling, manufacture, and testing with equipment in existing laboratory inventory. These requirements were both met by design of a sandwich with a one micron Thin Film bounded by and bonded to 6 millimeter thick Silicon substrate slabs to form a 6 mm x 12 mm compression test block. Figure 7 shows the developed test sample

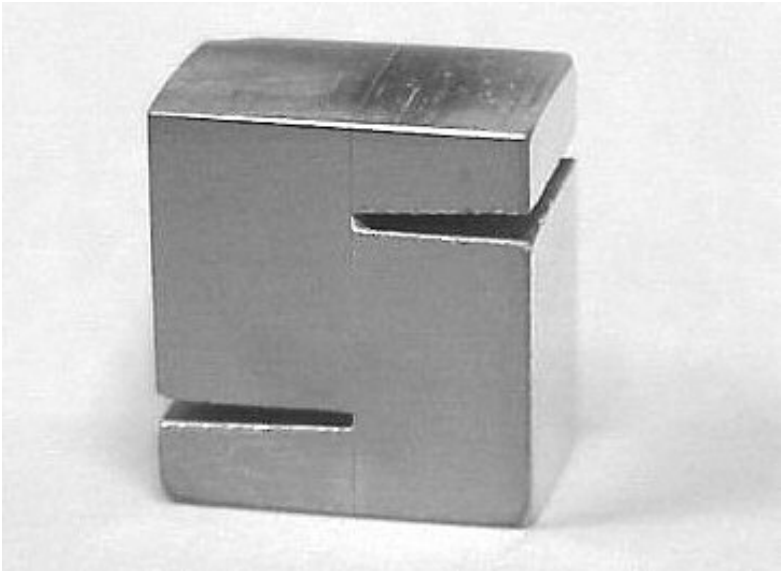

Figure 7. Manufactured test sample (side view) for isolating the PVD Aluminum Thin Film / Silicon interface in single shear. Sample is 6mm thick.

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1. Mechanical Design for Isolation of the PVD Thin Film / Substrate Interface

Single shear conditions are created on a 6 x 6 millimeter square face of the PVD Thin Film / Substrate interface by horizontal notching of the composite block. The First

notch is cut from the outer edge of the PVD side substrate to the PVD Thin Film / Substrate interface 2.5 millimeters from the bottom of the block. The second notch is cut from the DB side substrate through the thin film but not into the PVD side block. Each notch is 0.5 millimeter wide to allow for initial plasticity of the thin film and interfacial sliding creep with the block loaded in load control compression at high homologous temperatures. Figure 8 illustrates the design details in side view for a 6mm thick test sample.

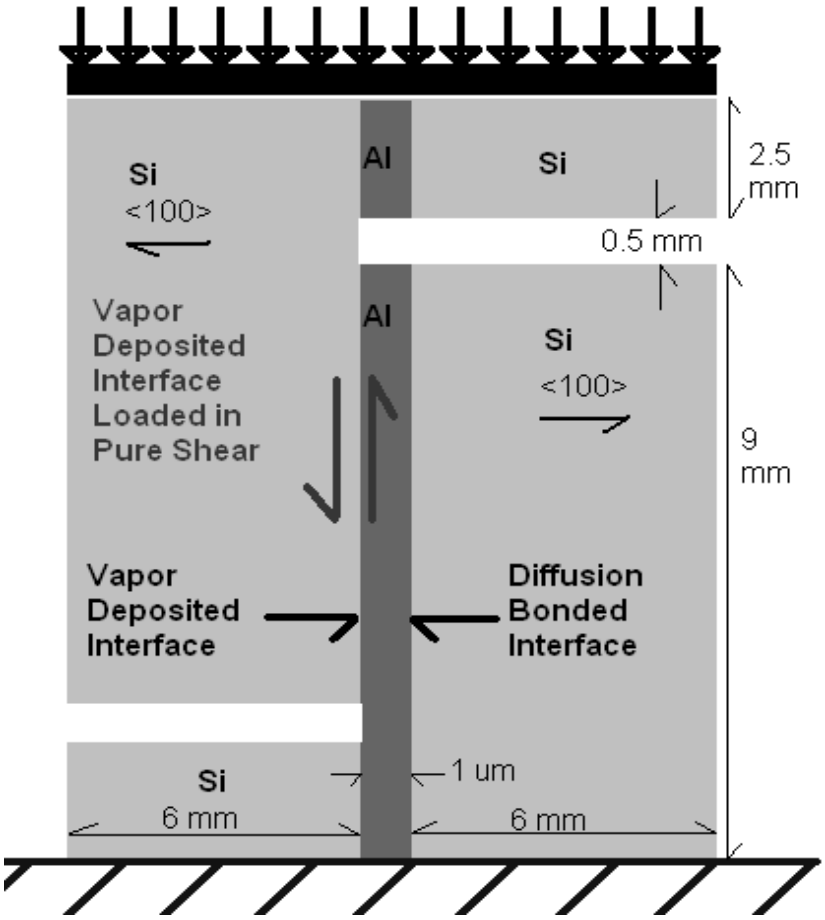

Figure 8. Designed test sample (side view) for isolating the PVD Aluminum Thin Film / Silicon interface in single shear. Sample is 6mm thick. Note: The Aluminum thin Film is not drawn to scale.

2. Material Selection

Samples were fabricated from 99.999+% pure single crystal Silicon, with the <100> direction pointing normal to the Thin Film interface. PVD Thin Film was created by PVD of 99.9% pure Aluminum to a 1 micron film thickness. The binary Phase diagram for the Al / Si system, Figure 8, shows very limited solid solubility at room temperature (~298 K) of either constituent. At the Eutectic temperature (850K) approximately 1.65 wt% of Si can dissolve into Al and approximately 0.5 wt% of Al can dissolve into Si. Thus forming a sharp interfacial region.

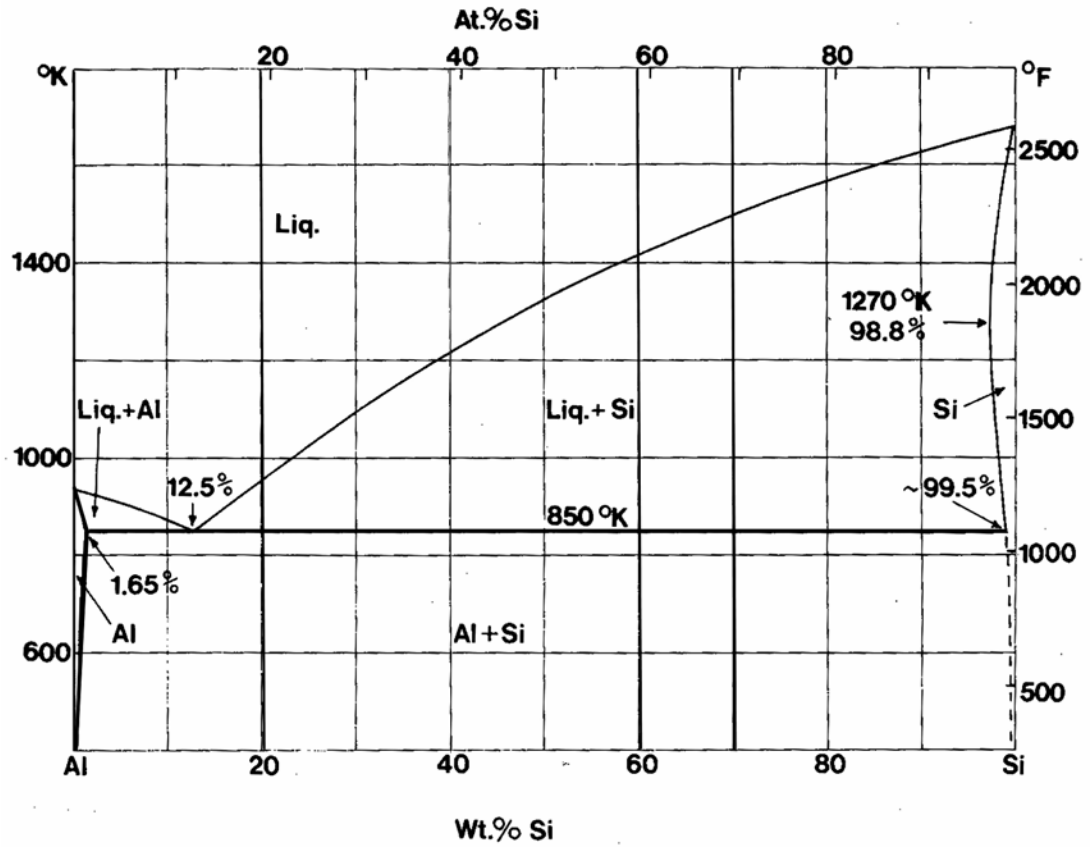

Figure 9. Binary phase diaghram for the Aluminum Silicon system. [From Ref 17]

The choice of Silicon as the substrate is relatively obvious as it is the predominant substrate material in use by industry to manufacture current generation microelectronic and microelectro-mechanical devices [16]. The choice of <100> orientation normal to the thin film was a function of the anisotropic etching step employed in final notching.

Aluminum was chosen due to its limited mutual solubility with Silicon [17] and its importance in current design microelectronics and microelectro-mechanical systems [16]. Figure 9 shows the Binary phase diagram for Silicon and Aluminum.

3. Fabrication

Fabrication of the test specimens involved a combination of traditional laboratory techniques and two leading edge technologies namely Diffusion bonding of a Silicon substrate / PVD Aluminum Thin Film / Silicon substrate composite and micro milling of Silicon with anisotropic TMAH etching solution. The following subsections detail the specifics of each major fabrication step in near chronological order.

a. Substrate Sectioning and Polishing

Pieces of silicon (28.5 x 28.5 x 6 mm) were sectioned from a four-inch diameter single crystal <100> Silicon ingot and polished to a 0.05μm finish on 1 square surface (interfacial surface) and 6.0μm finish on the other square surface (outer surface) using standard laboratory polishing techniques [2,7]. Figure 10 shows the orientation of the substrate section. Scratch orientation was maintained through the final polishing step to keep bond surface morphological orientation consistent with outer surface scratch orientation, enabling creation of a known surface morphology at the interface.

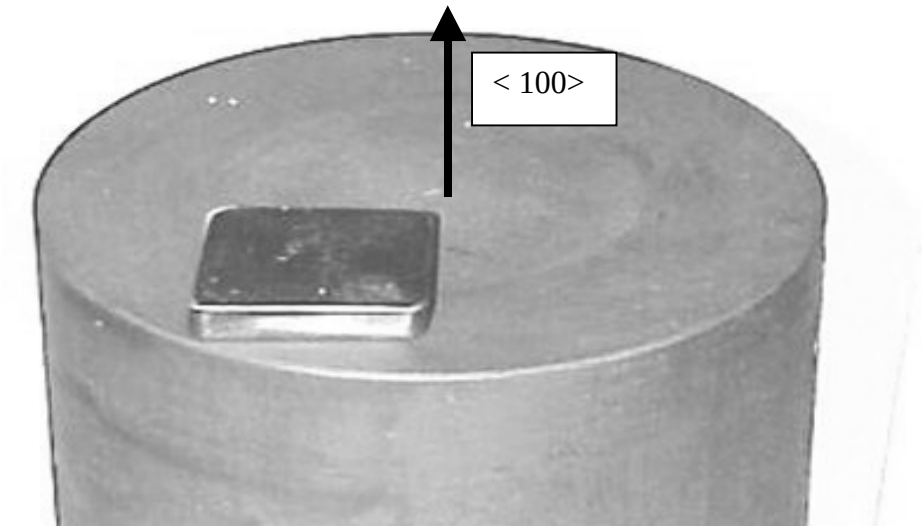

Figure 10. 28.5 X 28.5 mm sample block polished for PVD Al deposition. Surface morphology controlled by polish orientation during preparation stages.

The phenomenon of surface morphology is directly exploited in this experiment in that instead of a random polished surface the surface polishing was performed in deliberate steps and polish directions. Peterson, Dutta, and Chen [7] performed surface profile measurements by Atomic Force Microscopy (AFM) for both Si and Al samples prepared with progressively finer sized grit utilizing identical surface preparation techniques. These measurements were utilized to correlate the surface morphology of the substrate in the polished condition prior to bonding to the interfacial morphology (height (h) and period (λ)) of the bonded interface. Figure 11 shows the surface morphology measured for Silicon at progressively finer polishing stages [7].

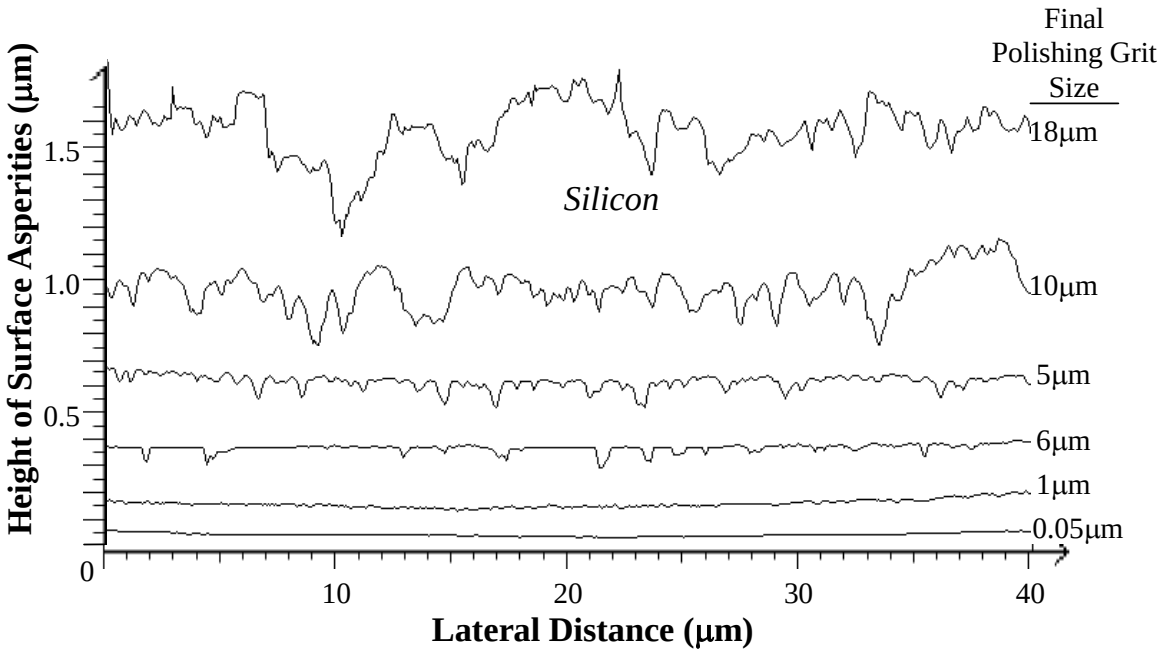

Figure 11. AFM Roughness Measurements on the Surface of Silicon after Using Various Grits and Grit Sizes During Final Polishing [From Ref 7].

The bonding or interfacial side of each Si piece was prepared to a 0.05 μm polished finish. Morphological orientation of the polished surface was tracked through the various fabrication stages to yield sample pieces having their "scratch orientation" running parallel to the bottom and top compression surfaces.

After mechanical polishing of the pieces they were cleaned in the series of steps shown in Table 1 prior to Film Deposition or Diffusion Bonding to minimize contamination of the interfacial surfaces.

1	2	3	4	5	6	7	8	9	10
Trichloro -ethylene Degrease	Acetone Degrease	Isopropyl Alcohol Dry	De-ionized H_2O Rinse	H_2SO_4 Oxidize	De-ionized H_2O Rinse	10% HF De-oxidize	De-ionized H_2O Rinse	Ethanol Rinse	Dry in Hot Air
4min	4min	4min	10min	2 hr	10min	2min	10min	2min	5min

Table 1. Cleaning Sequence for Surfaces of Si Prior to PVD of Al thin film and Mating with PVD sample for Diffucion Bonding.

Initial anticipated yield from each pair was 8 test samples. However, surface curvature of the square surfaces was not measurable with equipment in our laboratory below 10 microns of arc difference center to edge of the specimen. This inaccuracy reduced actual yield to 2-3 test samples per pair. In a later trial several prepared (28.5 x 28.5 x 6 mm) pieces were quartered to (14 x 14 x 6 mm) and re-polished to a 0.05μm finish on the bond surface for reasons to be discussed under diffusion bonding. These later pieces produced a yield of 2 test samples.

b. PVD Thin Film Deposition

The metallic thin film interface was formed by Physical Vapor Deposition (PVD) of a 1 μm Aluminum film on a section of polished Silicon substrate. To accomplish this deposition polished silicon sections 28.5mm square by 3 mm thick were fastened onto a heated sample holder and placed in the PVD vacuum chamber. Vacuum was drawn to $2x10^{-7}$ torr and stabilized for 12 hrs at room temperature. Substrate temperature was increased at the rate of 10 K per minute to 573 K then held for two hours to remove any residual surface contamination. At completion of the 2 hr heat run temperature was dropped at the rate of ~1 K per minute to 423 K. Evaporative Deposition from two source coils of Tungsten wire filled with 99.9% pure Al chips was performed, while holding substrate temperature at 423 K, to produce a 1 μm thin film on

the bond surface of the sample as measured by ultrasonic thickness monitor. Film deposition was performed with vacuum at $2x10^{-6}$ torr and deposition rate maintained between 6 and 10 nm per minute with 23-25 amps of current (to maximize life of the tungsten source coils). A moveable shutter was employed to protect the Si surface from any contaminants or oxides on the Al chips. Vapor deposition was started with the Aluminum shutter in place. After 25-40 nm of relative deposition the shutter was rotated to expose the Si surface and enable deposition to occur. The actual amount of deposition from each basket load of Al chips varied from 300 to 700 nm. By utilizing two source baskets the first basket of evaporation is allowed to complete then the shutter was rotated back into a protective position until again 25-40 nm relative of Al had been released from the second basket. After which the shutter is again rotated and deposition allowed to occur. Note that while a single ultrasonic thickness probe was utilized a two-channel monitor was employed with each channel calibrated to the slight geometric differences between source, target and probe. Figure 12 shows a diagram and picture of the component geometry utilized within the PVD vacuum chamber.

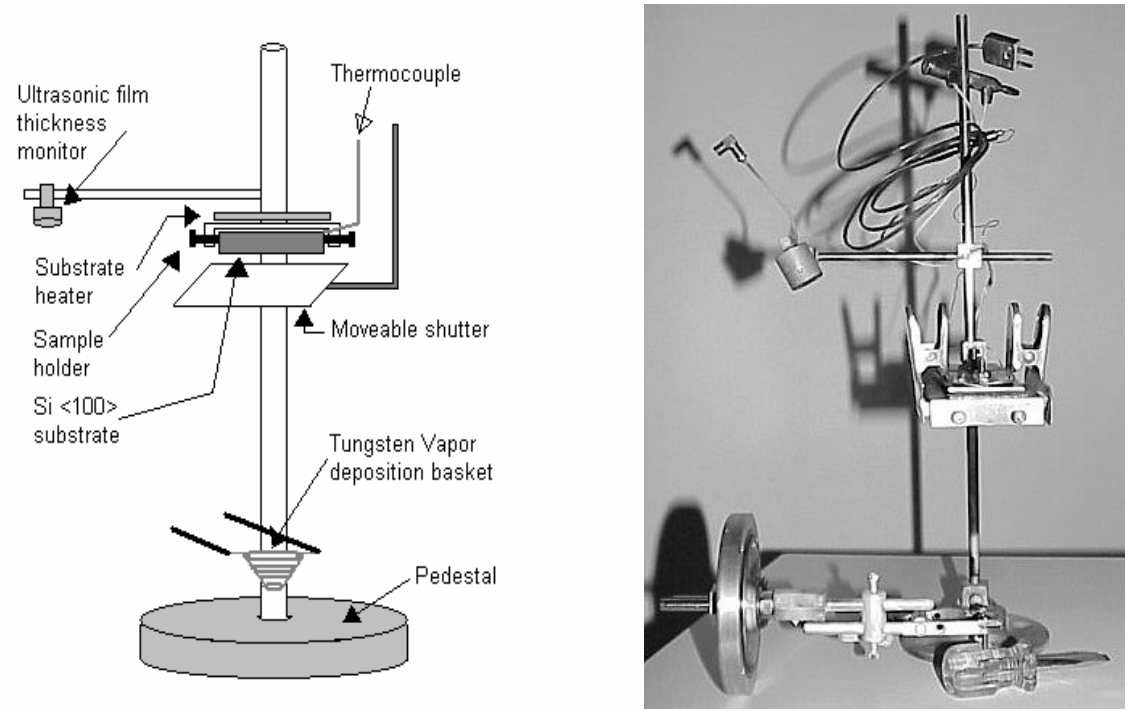

Figure 12. PVD chamber internal orientation for Al thin film deposition on polished <100> Si substrate pieces note; shutter not shown in picture..

At completion of film deposition the samples were heated to 623 K for 15 minutes to promote diffusion bonding at the interface and stabilize the film microstructure then allowed to slow cool to ambient temperature. Upon removal from the PVD chamber film covered pieces were mated with cleaned polished pieces (being careful to match surface morphology and orientation), wrapped tightly in Aluminum foil, and stored under vacuum or moved immediately into the diffusion bonding vacuum chamber to minimize oxidation.

c. Diffusion Bonding

Diffusion bonding of a second Silicon substrate section to the exposed surface of the PVD Aluminum thin film was performed to create a Silicon substrate / Aluminum thin film / Silicon substrate composite sandwich. The orientation of components and their placement within the diffusion bonding press were controlled for interface tracking and interfacial morphological alignment matching. Sample pairs wrapped in Aluminum foil were placed between 1 mm thick Aluminum buffer plates and inserted into a high strength steel die lubricated with Molybdenum DiSulfide (MoS_2). The die was then immediately placed into the bellows vacuum chamber of the diffusion bonding press and vacuum drawn. Figure 13 shows the internal arrangement of the diffusion bonding press.

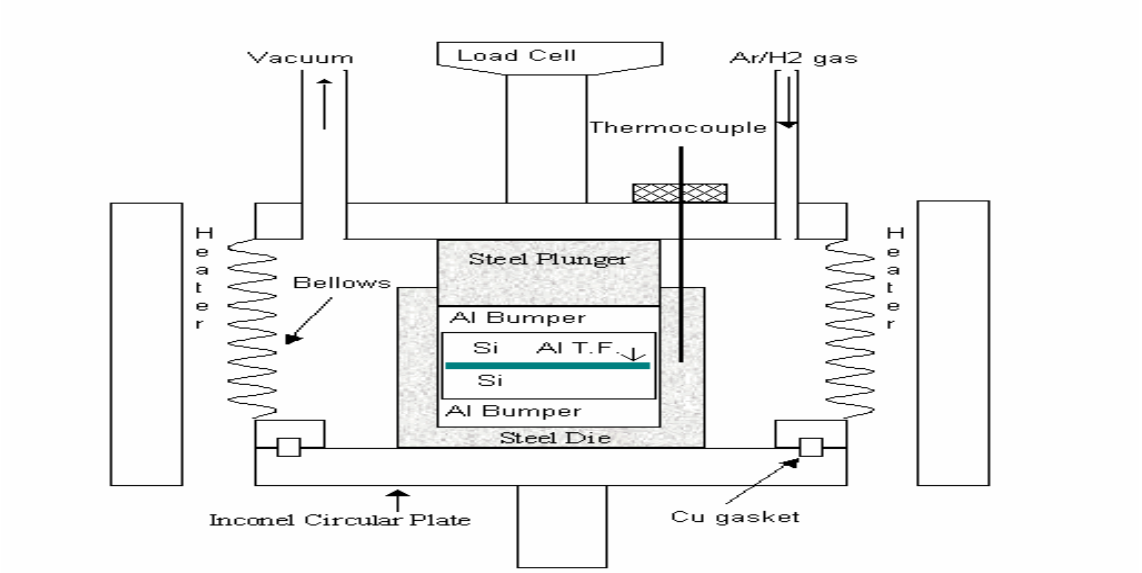

Figure 13. Diffusion bonding chanber orientation and arrangement for diffusion bonding PVD Al Thin Film to polished <100> Silicon to form final composite test specimens.

Once the die was inserted and bellows made up vacuum was drawn to $2x10^{-2}$ torr and three cycles of Argon purging were performed to minimize residual oxygen within the chamber. Vacuum is then increased to $2x10^{-5}$ torr and an initial pre-load of 150 N placed on the sample. Heat was raised at 2 K per minute to 838 K with care to not overshoot and stabilized. Once thermal conditions were met the sample was loaded, at the rate of 10 N per minute, to 4 MPa and held for 2 hours. After the 2-hour bonding period heat and load were ramped down linearly over a period of 8 hours returning to 298 K and 75 N. These conditions closely match the conditions for Diffusion bonding of bulk Aluminum to polished Silicon previously determined [7]. Figure 8, shown previously, and Table 2 provide further details on the material properties of each constituent.

	Silicon	Aluminum [60, 61]
Melting Temperature (K)	1683	933
Crystal Structure	Diamond Cubic	Face Centered Cubic
Hardness (GPa) @ 298K	13 [102]	0.08
Yield Strength (MPa)	--	
@ 298K		34
@ 673K		5
@ 847K		~1.5
Coefficient of Thermal Expansion ($x10^{-6}$ K^{-1})	2.35	25.5

Table 2. Physical Properties of Al and Si Relevant to Diffusion Bonding [From Ref. 7].

The conditions noted in the previous paragraph failed to produce fully bonded (28 x 28 mm) pairs, producing on average a (18 x 18 mm) region of good bond as determined by intentional breaking of scrap edges during dicing. Many sample pairs were utilized in attempting to improve the bonded area. After much analysis it was concluded that the surface contour inherent in the polished Silicon pairs was precluding establishment of a contact surface for diffusion outside of this area. Figure 14 shows the central region of good bond surrounded by a region of incomplete bonding. This composite piece was intentionally fractured by application of opposing torque to the Silicon substrate sections.

Figure 14. Picture of partially bonded composite specimens (after intentional fracture) showing area of diffusion bonding center with region of inadequate surface contact (failing to produce viable diffusion bonding) in peripherary region.

This produces a yield of 2-3 test samples vice the intended 8. One trial was made with a quartered (14 x 14 mm) sample pair resulting in a fully bonded (14 x 14 mm) region producing a yield of 2 test samples per intended 2. Figure 15 is a micrograph of the composite from a section within the good bonded region. It shows the retained integrity of the 1μm Aluminum thin film post diffusion bonding.

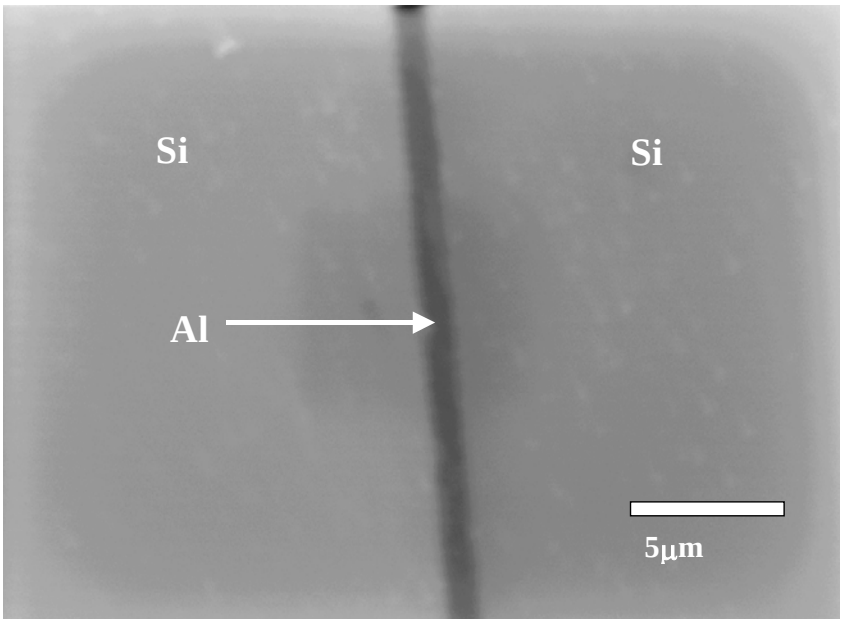

Figure 15. Si / Al thin film / Si composite showing retained integrity of the 1μm Aluminum thin film following duffusion bonding.

Of the bonding runs performed the following information is pertinent. Bonding Stress in excess of 4 MPa is unnecessary. All samples subjected to stresses greater than 4 MPa experienced some cracking, most catastrophically. Bonding Stress of 2 MPa or less produced an appreciably smaller area of good bonding than that produced at 4 MPa. Bonding Temperatures below 834 K produced no bond whatsoever (2 of 2 tries). Bonding temperatures above 838 K are dangerously close to the eutectic temperature Bonding at 841 K resulted in the film becoming eutectic.

d. Dicing

Dicing of sample pieces was performed with a slow speed diamond wafering saw modified to accommodate a table and guide rail with a secondary motor controlled feed. This modification minimized cutting stress on the pieces during dicing and improved the linearity and accuracy of cuts performed. Dicing of bonded pairs was originally intended to trim 2 mm from the edges of the (28 x 28 mm) bonded pairs then subsection the remaining region into 8 (12 mm tall x 6 mm wide x 6 mm thick) test samples. Figure 16 shows the dicing plan employed. Figure 17 is a picture of a specimen being diced.

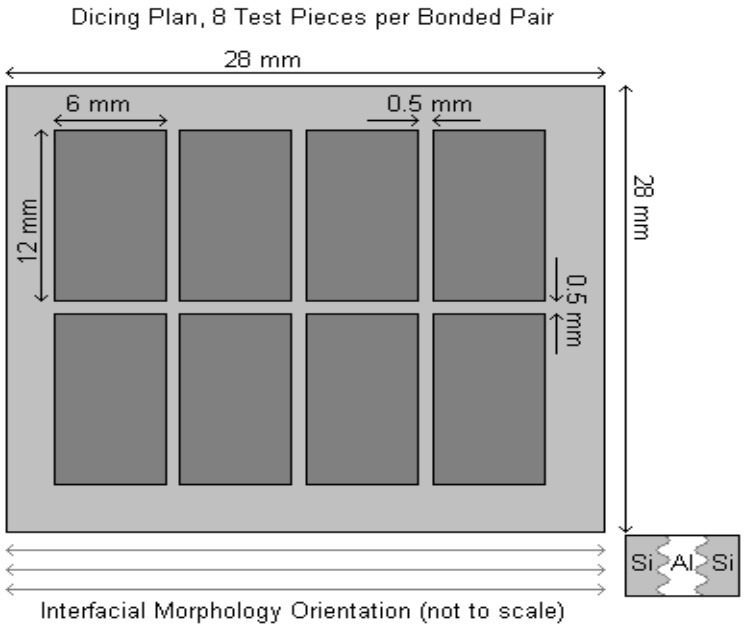

Figure 16. Dicing plan to produce 8 test samples per ~28mm X 28mm composite section.

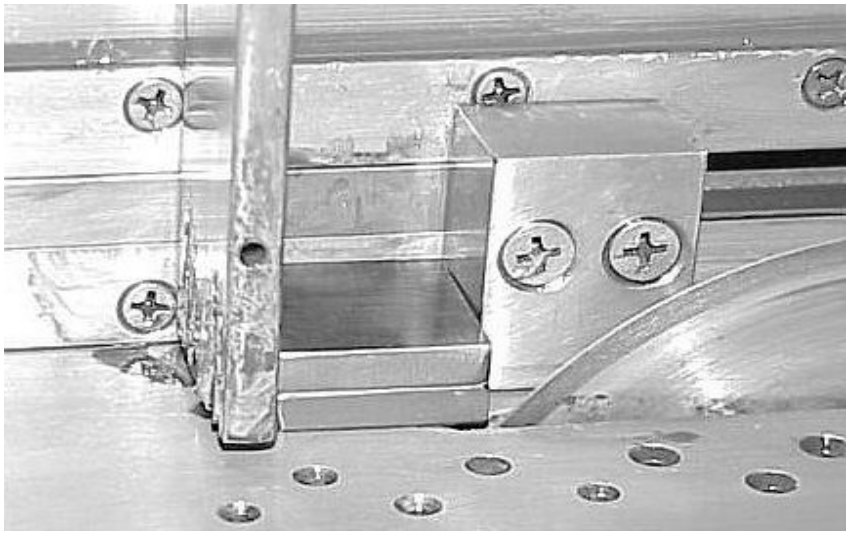

Figure 17. Dicing of 28 X 28 mm composite pieces to produce 6 X 12 mm test pieces. Dicing performed on modified diamond wafering saw with controlled feed to minimize stresses during sectioning..

As the 2 mm wide pieces were cut from the original composite sample they were intentionally broken to check for evidence of good bonding (Silicon fracture vice film de-bonding at the interface). If not found to be well bonded additional slices were removed until the region of strong bonding was entered along the entire periphery of the composite sample material. The remaining material was diced into appropriately sized and oriented samples as the material allowed while maintaining the desired morphological orientation.

e. Notching

Notching of the sample was performed by diamond wafer saw. Multiple passes were performed taking initially 1 mm of cut depth then decreasing with each cut as the interface is approached until the notch cut distance to the interface is approximately 200 μm from the interface. Figure 18 illustrates the wedge apparatus employed with the standard wafering saw to vary the cut depth enabling incremental approach to the interface while minimizing stress on the test specimen. Figure 19 shows an optical micrograph of the notch tip after notching with the diamond saw.

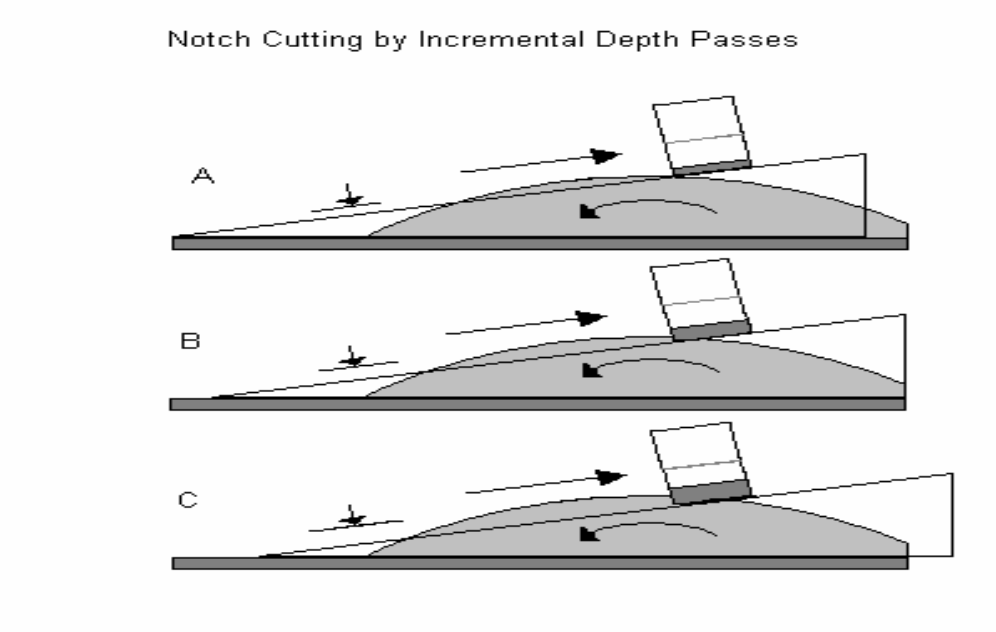

Figure 18. Notch cutting on modified diamond wafering saw to produce initial notching of test specimens. Repeated passes at greater depth but reduced material engagement thickness performed to minimize stresses during notching process.

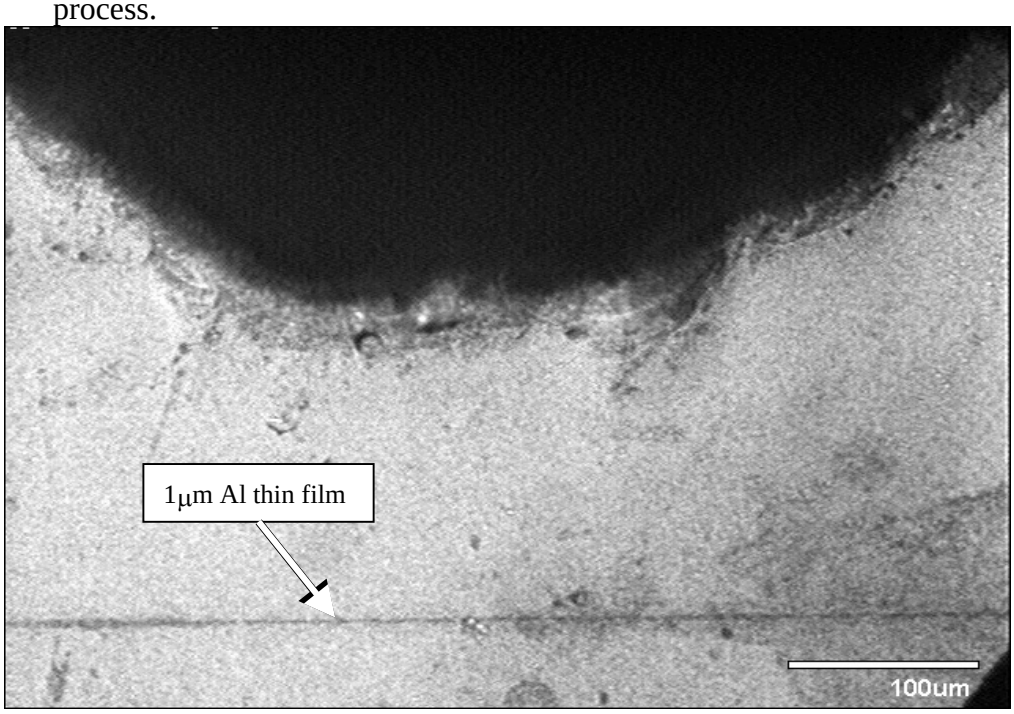

Figure 19. Picture of notched specimen prior to final notch etching. Notch depth ~200um short of the Al Thin Film interface

Following diamond saw cutting the notches were gently hand filed using a diamond flat file (mfg from a worn out diamond wafering blade) until both notches were approximately 150 μm from the interface through the sample thickness and the same distance from the interface at both notches as observed periodically under a stereo optical microscope.

f. Masking

Masking of the notched specimens was performed to protect the un-notched sections from bulk etching during the final notch etching process. Two methods of masking the external sample surfaces for notch etching were investigated. The first method tried was to grow a passive silicon oxide layer of approximately 0.15 μm thickness, as indicated by a light to metallic blue surface color under daylight fluorescent lighting [16]. This was performed by heating the pieces from ambient to 823 K at ~ 1 K per minute then baking the pieces for 2 hours in a tube heater with wet flowing O_2 followed by cooling to ambient at ~ 1 K per minute. The SiO_2 layer proved to be durable during etching but provided less protection for the Aluminum rich diffusion layer (on both sides of the film) than desired. The second method employed was to PVD a 500 nm layer of Aluminum to the exterior of the piece. This second method provided excellent surface passivation but was soft and weakly diffusion bonded to the surface. It did appear that coalescence during vapor deposition caused a thicker layer over the Aluminum Film which aided in visually tracking etch depth during etching but abrasion with the sample basket caused much of this film to be removed during the course of the etching process as evidenced by tiny flecks of Aluminum swirling in the etch solution. The most successful masking was achieved with a combination of the two masking systems. The first forming the SiO_2 layer then depositing a ~ 500 nm Al thin film over the SiO_2 layer. After masking the entire sample the passive layers are removed from the notch tip by a second round of gentle filing with the diamond file to expose un-oxidized Silicon at the notch tip then immediately placed in the etch solution.

g. Etching

Notching of the sample to the depth of the Aluminum film but not damage the Aluminum film is not possible with purely mechanical means. For this step anisotropic etching of the Silicon is desired without attacking exposed Aluminum. A recent development in microelectro-mechanical fabrication technology in utilizing TetraMethylAmmonium Hydroxide (TMAH) in chemically milling the remaining notch was employed [18]. The etchant utilized was 5 wt% TMAH ($(CH_3)_4NOH$), 1.5 wt% dissolved Silicon (Si) and 0.5 wt% Ammonium Peroxidisulfate ($(NH_4)_2S_2O_8$). On flat surfaces at 358 K this etchant produces anisotropic etch rates of <100> Si of 0.9 μm/min., Al 0 μm/hr., and SiO_2 70 nm/hr.

There are drawbacks to employing this etchant to chemically mill the channels. First, at temperatures of about 358 K a white polysilicate gel precipitates out of solution [18] and appears to clog and mask the very channel attempting to be etched. Second, etching of the Silicon produces Hydrogen gas bubbles [18], which also tend to mask the surface attempting to be etched. And Third, exposure to air for even very short periods of time causes immediate growth of 10-20 angstroms of SiO_2 on the surface [16, 18] which takes approximately 2 hours to etch through, thus making it difficult to check the progress of etching under an optical microscope (for every check made approximately 2 hours of etching are required to begin further etching of any appreciable amount).

Several methods of etching were tested. Initially the etchant was mechanically pumped through a nozzle directly into the channel that worked initially well but after several cycles of etchant were pumped through the channel precipitate began coming out of solution in the pump, piping, and at the nozzle. Although the polysilicate precipitate was readily cleaned any stop in the etching allowed SiO_2 growth to occur delaying the time required to complete etching. Bulk etching in a beaker produces excellent exposed surface results but the channel desired to be etched allows for coalescence of H_2 bubbles and readily fills with polysilicate precipitate both of which self-mask the channel. Suspension of the piece in stirred 363 K etchant yields the best result to date. Flow through the channel is improved reducing the extent of self masking but not eliminating it. Periodically (3-5 min. every 30 min.) removing the sample from

the etchant and placing it in 363 K stirred deionized water tends to clear the build-up of polysilicate from the channel provided that the sample's channel is not exposed to air while switching between etchant and the water produces a channel etch rate of 0.2 μm/min. This is only one quarter the flat surface etch rate (observed in several unmasked test samples) but it is sustainable. Figure 20 shows the in-lab apparatus employed to perform TMAH etching..

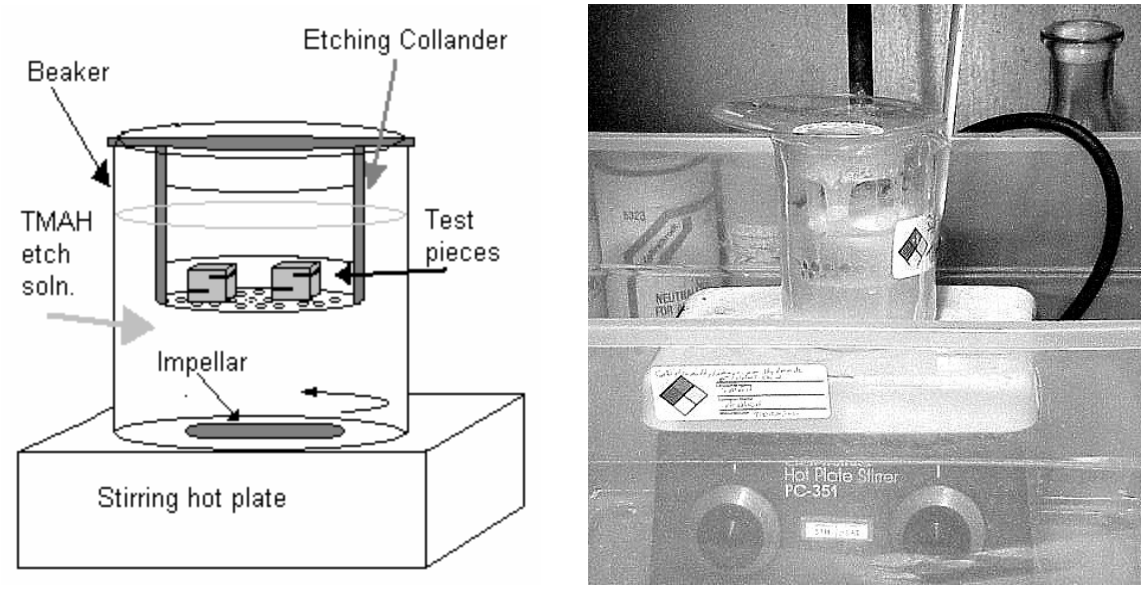

Figure 20. Final milling of notch channel via TMAH etching. Etching was performed in stirred TMAH at 359 to 363 K. Stirring helped to minimize self masking in the etch channel due to polysilicate precipitate and Hydrogen bubble formation.

Stirring the etchant more forcefully should improve this etch rate but there are problems. One attempt to stir the etchant more forcefully resulted in ejection of several samples from the etching colander platform and resulted in them impacting the flow impeller at the bottom of the beaker. A second attempt at stirring more vigorously with a higher walled etching colander resulted in entrainment of the sample pieces with the swirling TMAH and mechanical abrasion of the sample surfaces with the etching colander wall. This abrasion damaged the Aluminum film protective mask and resulted in uneven loss of the protective mask of the non-notch surfaces.

After etching the side faces of the test samples were lightly polished to remove the passive Al film while retaining the film on the compression faces. Continuity of the thin film was measured by a Fluke 8600a digital multimeter and the resistance was shown to be less than one ohm. Finally the notch on the Diffusion Bonded side of the sample was etched through the Aluminum film utilizing a thread wetted with 10% Hydroflouric Acid (HF) rubbed across the film for 10 seconds then thoroughly flushing the etch channel with DI water. After etching through the Al film on the DB side notch continuity was measured and found to be greater than 10 K ohms indicating removal of the Al from the Diffusion Bonded side notch.

B. TESTING APPROACH

The overall objective, of which this work is a part, is to parameterize and validate through testing the kinetics of interfacial sliding of Aluminum thin film / Silicon substrate interfaces. A significant part of this effort lies in the design of the experimental apparatus upon which the test samples, when fabricated, can be tested. The experimental apparatus and test sample are linked in that the design of both must be compatible with each other in order to obtain a workable result [19]. To that end the test apparatus was designed, fabricated, and aligned with specimen blanks in preparation for testing. Figures 21 and 22 illustrate the designed and fabricated test stage.

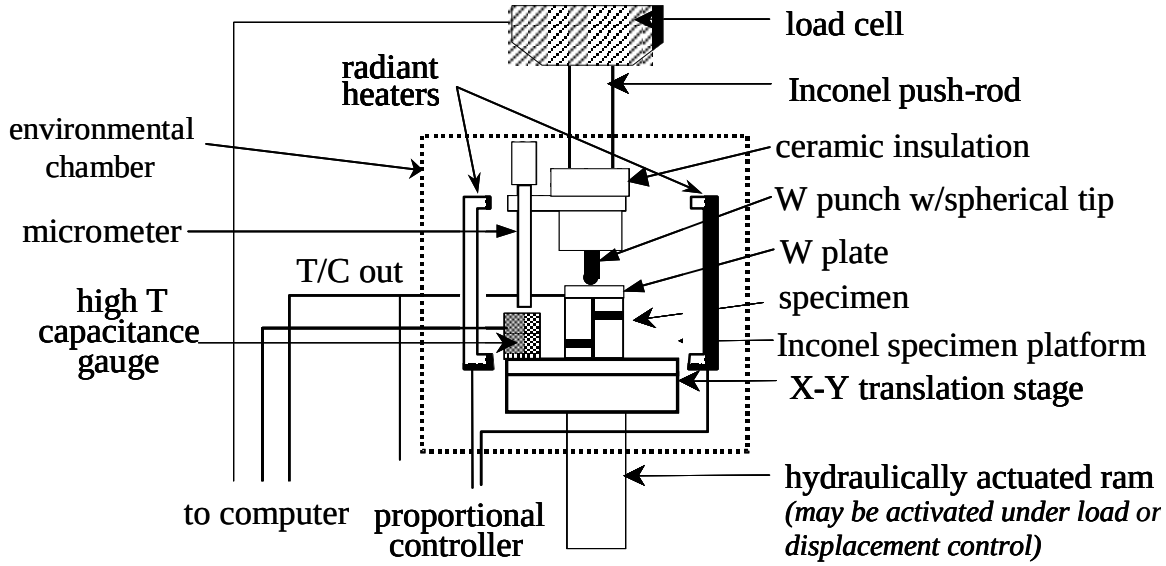

Figure 21. Design of test stage for isolated single shear loading of the PVD Aluminum Thin Film / Silicon interface.

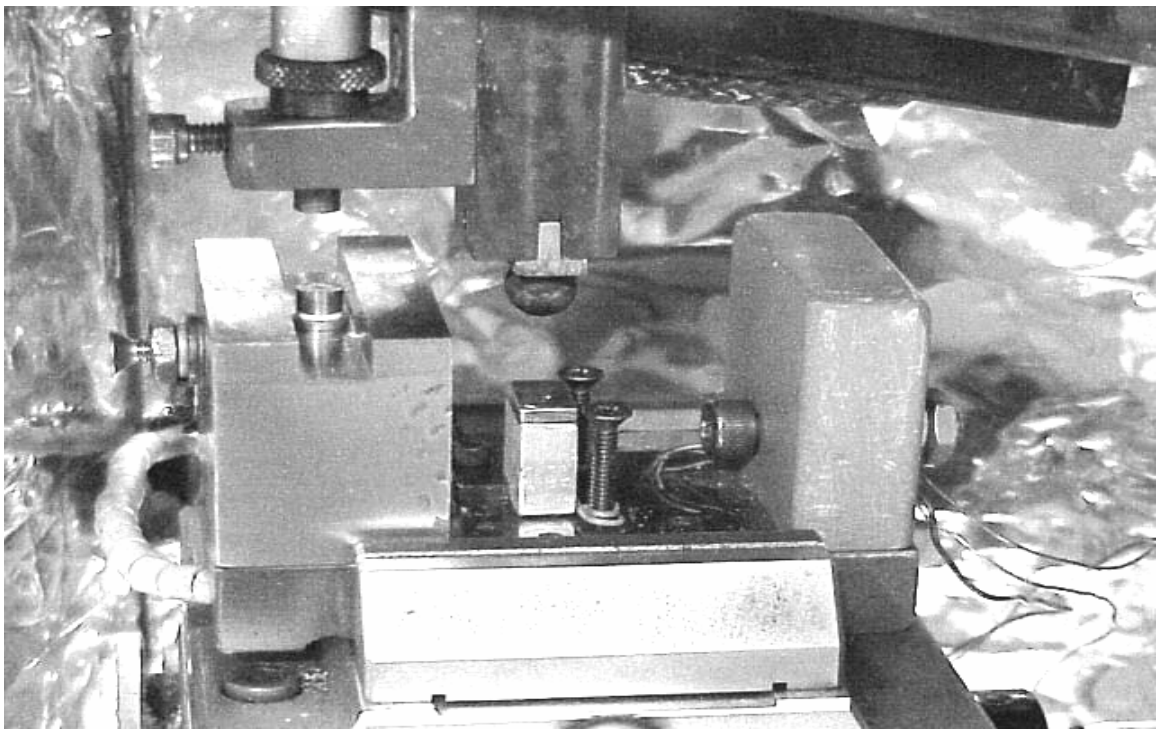

Figure 22. As built configuration of test stage. Test specimen pictured is a pure Aluminum block (of the same external dimensions as the Interfacial sliding test specimens) utilized in pre-test calibration of test equipment.

1. Test Condition Requirements

Testing of the interfacial sliding creep requires two principle conditions to be met and maintained steadily for long periods of time and must allow for the smooth transition of the test sample from its initial state to the test state in such a way as to minimize the effect of unintended stress interactions from skewing the results. The two conditions to be maintained are steady temperature at a high homologous temperature and steady load in the presence of sample movement as a response to the applied load.

Meeting the temperature requirements required establishing steady thermal control at high homologous temperatures for Aluminum. To accomplish this, two factors had to be controlled; heating of the stage and thermal isolation of the stage from the laboratory environment. To control heating a pair radiant of heaters were powered from a proportional power controller with insitu thermocouple feedback from the stage. Isolation of the stage from laboratory ambient was performed in three layers. The inner layer comprised the walls directly surrounding the stage of which the heating elements formed two walls the stage itself formed the floor and 1.5 cm thick ceramic blocks formed the walls and roof with exception of the opening for the load cell shaft and capacitance gage micrometer. The second layer was formed with 2 cm thick fiberglass sheet insulation wrapped in foil for radiant shielding and dust control. The outer layer comprised a layer of thermal bricks below the stage and the walls of the environmental enclosure. This resulted in being able to maintain temperature $300 \pm 0.15^{o}C$ over a 40-hour period following controller calibration. In changing temperature the controller was calibrated to achieve a $0.75^{o}C$/min. heat-up rate with cutback control to limit overshoot excursions to less than $4^{o}C$ on heat up from ambient to $300^{o}C$.

Load control was accomplished via MTS programming to maintain load ± 0.2 N at 72 N load with a creeping Aluminum test blank and to limit load excursion on initial loading to 0.3 N maximum excursion deviation from prescribed load.

2. Load Application

The creep range over that the sample is anticipated to be tested results in overall compression of the sample on the most limiting test of 200 μm. Accurate deflection

measurement in this range while at high homologous temperatures necessitates the employment of a capacitance gage housed in a material insensitive to the application temperatures. For this test a capacitance gage housed in Inconel X-750 was employed which has negligible thermally induced deviation over the range of testing. The Load cell shaft is also critical as its length is appreciable. This shaft was fabricated from Invar 36 which has a near zero coefficient of thermal expansion over the intended test temperature range. Coupling the Load Cell shaft to the Capacitance Gage was performed by a locking micrometer that provided adjustability to accommodate variance in test sample height without sacrificing usable range of the capacitance gage. Coupling the Load Cell to the sample was performed via a Tungsten ball and 2mm thick Tungsten plate that provided for uniform load distribution over the top of the test sample in the presence of sample upper surface parallelism variance with the test stage. A 0-500 lb calibrated load cell provides for loading measurement.

3. Testing Matrix

Sample testing is intended to provide experimental data from which the proposed model fit can be determined and from which full kinetic parameterization of the model can be performed to provide a substantiated and characterized description of the observed phenomena of interfacial sliding creep for PVD thin film / Silicon interfaces. Kinetic parameterization of this phenomena is anticipated to be of value in the development of current and future generation microelectronic and microelectro-mechanical systems. To characterize this model properly testing must be performed over the region of primary concern namely the range of high shear stress and high homologous temperatures where the observed phenomenon is of greatest concern for the fabrication and long-term reliable operation of these components. A test matrix has been developed for this intended region from which that data necessary to perform a meaningful characterization of the phenomenon can be performed within the limitation of the samples developed and the range of validity of the designed test equipment. Table 3. itemizes the proposed tests for parameterization of PVD Aluminum Thin Film / Silicon Interfacial Sliding Creep. Each proposed test to be repeated as necessary to generate the appropriate student's distribution confidence interval for parametric characterization of the proposed model.

Test	Temp (^{o}C)	Temp (K)	Temp (Homologous)	Shear Stress (MPa)	Load (N)
1	200	473	0.556	1.5	108
2	250	523	0.615	1. 5	108
3	300	573	0.674	0.5	36
4	300	573	0.674	0.75	54
5	300	573	0.674	1.0	72
6	300	573	0.674	1.25	90
7	300	573	0.674	1.5	108
8	300	573	0.674	1.75	126
9	350	623	0.733	0.5	36
10	350	623	0.733	0.75	54
11	350	623	0.733	1.0	72
12	350	623	0.733	1.25	90
13	350	623	0.733	1.5	108
14	350	623	0.733	1.75	126

Table 3. Test Matrix for Parametric Characterization of PVD Aluminum Thin Film / Silicon Interfacial Sliding Creep

V. SUMMARY

This thesis developed the sample design and testing methodology for parametric characterization of Interfacial sliding in a thin film – substrate system based on evaporated Al on Si. Test samples were designed and fabricated to enable loading of the Al thin film – Si substrate interface in simple unidirectional shear, while ensuring that the measured displacement between the two sides of the sample truly reflect the interfacial sliding displacement in isolation from deformation of the Al thin film. Test sample fabrication development resulted in three successful applications of emerging technology. First a methodology of diffusion bonding bulk Silicon and Aluminum segments was optimized to successfully diffusion bond a Silicon substrate to a 1 μm Al thin film evaporated onto a second Silicon substrate while retaining the integrity of the Aluminum thin film. Second a masking and etching scheme was devised to enable deep anisotropic etching of a deep and narrow channel in <100> Silicon of an Silicon / Aluminum thin film / Silicon composite while retaining the integrity of the composite piece away from the channel during a prolonged etch process. And third a simple method of etching a deep and narrow channel in <100> Silicon by reduction of inherent self-masking effects was shown to be viable in the basic laboratory environment. The test samples developed are reproducible using in-house equipment and processes in our laboratory. These samples are also of a size amenable to handling and testing on in-house equipment. In conjunction with the sample development a test platform was designed, fabricated, assembled, and aligned to provide for isolated parametric characterization of the interfacial creep kinetics of a PVD metallic thin film on a Silicon substrate. The results of this characterization are anticipated to be of significant utility in improving the design for fabrication and reliability of current and next generation microelectronic and microelectro-mechanical devices.

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